BLG222E Computer Organization

Project 2

Group Members (representative in bold):

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List of control inputs and corresponding functions for our design:

Part-1:

Inside the ALU.

Inputs:

* Input: 8-bit I
* CLK: Clock
* FunSel: Selects which function should be applied (4 bit)
* Cin: Carry in.

Outputs:

* Output: OutALU
* OutFlag: ZCNO
* Z: Zero
* C: Carry
* N: Negative
* O: Overflow

Part2:

Inside the Project 1 part2a (Register File).

Inputs:

* Input: 8-bit I
* OutASel: Register selector for OutA output
* OutBSel: Register selector for OutB output
* RegSel: Selects which register(s) should be operated upon by FunSel
* FunSel: Selects which function should be applied
* CLK: Clock signal

Outputs:

* OutA: Output A decided by OutASel
* OutB: Output B decided by OutBSel

|  |  |  |  |
| --- | --- | --- | --- |
| OutASel | OutA | OutBSel | OutB |
| 00 | R0 | 00 | R0 |
| 01 | R1 | 01 | R1 |
| 10 | R2 | 10 | R2 |
| 11 | R3 | 11 | R3 |

Inside the Project 1 part2b (Address Register File).

Inputs:

* Inputs: 8-bit I
* FunSel: Selects which function should be applied
* RegSel: Selects which register(s) should be operated upon by FunSel
* CLK: Clock signal
* OutCSel: Register selector for OutC
* OutDSel: Register selector for OutD

Outputs:

* Output C: Output C decided by OutCSel
* Output D: Output D decided by OutDSel

|  |  |  |  |
| --- | --- | --- | --- |
| OutCSel | OutC | OutDSel | OutD |
| 00 | R0 | 00 | R0 |
| 01 | R1 | 01 | R1 |
| 10 | R2 | 10 | R2 |
| 11 | R3 | 11 | R3 |

Inside the Project 1 part2c.

Inputs:

* /H: Selects at which bits (0-7) on low, (8-15) on high should input be loaded
* Input: 8-bit input
* CLK: Clock signal
* Enable: Enable Input (E)
* FunSel: Selects which function should be applied

Outputs:

* out0-out15: 16-bit Output

|  |  |  |  |
| --- | --- | --- | --- |
| /H | Enable | FunSel | IR+ |
| ɸ | 0 | ɸɸ | IR |
| ɸ | 1 | 00 | 0 |
| ɸ | 1 | 01 | IR + 1 |
| ɸ | 1 | 10 | IR – 1 |
| 0 | 1 | 11 | IR(0-7) <= I |
| 1 | 1 | 11 | IR(8-15) <= I |

Inside the ALU.

Inputs:

* Input: 8-bit I
* CLK: Clock
* FunSel: Selects which function should be applied (4 bit)
* Cin: Carry in.

Outputs:

* Output: OutALU
* OutFlag: ZCNO
* Z: Zero
* C: Carry
* N: Negative
* O: Overflow

Inside the MuxC.

Inputs:

* MuxCSel
* MuxASel output
* Register File OutA

Outputs:

* MuxC output

Inside the MuxA.

Inputs:

* MuxASel
* OutALU
* IR(0-7)
* Memory output
* Address Register File Output

Outputs:

* MuxA output

Inside the MuxB.

Inputs:

* MuxBSel
* OutALU
* Memory Output
* IR(0-7)

Outputs:

* MuxB output

Inside the Memory.

Inputs:

* OutALU
* Address: Address Register File Output

Outputs:

* Memory output